A −119.2 dBc/Hz at 1 MHz, 1.5 mW, Fully Integrated, 2.5-GHz, CMOS VCO Using Helical Inductors

Joonho Gil, *Student Member, IEEE*, Seong-Sik Song, *Student Member, IEEE*, Hyunjin Lee, and Hyungcheol Shin, *Senior Member, IEEE*

***Abstract*—This letter presents the implementation technique to reduce area occupation in designing voltage-controlled oscillators (VCOs) using filtering technique. We applied a helical inductor to the noise filter in 2.5-GHz CMOS VCO to reduce area occupation. Because a helical inductor has less area occupation, small silicon area was achieved. This VCO is operating in the 2.5-GHz band with power consumption of 1.5 mW and phase noise of −119.2 dBc/Hz at 1-MHz. Our VCO has the excellent performance of the phase noise over the power consumption.**

***Index Terms*—CMOS, helical inductors, phase noise, RF, voltage- controlled oscillators.**

I. Introduction

MANY design challenges may be faced toward a CMOS single-chip radio. Among them, to design an integrated CMOS voltage-controlled oscillator (VCO) with low phase noise, low power consumption, and low cost is important issue. From this point of view, a filtering technique [1] is one of solutions to lower the phase noise of the VCO without additional power consumption. The only drawback of a filtering technique is a large area occupation due to additional inductors, and therefore there is tradeoff between low phase noise and small area occupation.

In this letter, using helical inductor [2] for a noise filter is proposed to reduce area occupation. A 2.5-GHz CMOS VCO using helical inductor was fabricated in a 0.18-μm 6-metal CMOS process. Because a helical inductor has less area occupation, small silicon area was achieved. This VCO is operating in 2.5-GHz band with low phase noise and low power consumption.

II. VCO Design Using Helical Inductors

Helical inductor occupies less silicon area than that of planar spiral since the turn is expanded vertically as shown in the insert of Fig. 1, [2]. Fig. 1 shows the measured quality factor and inductance of helical inductors with various number of turns. The measured inductance and Q-factor at 5.2-GHz for 4-turn helical inductor were 1.9 nH and 7, respectively. Generally, top metal is thicker than the other metal layers, so Q-factor of helical inductor would be worse than that of planar spiral. However, the area occupation of helical inductor is much smaller. In addition, smaller area occupation gives smaller substrate loss, so little performance degradation of the helical inductor over the planar spiral is expected. Consequently, helical inductors can be applied to applications that small area is required such as noise filters in VCOs, source degeneration inductors in LNAs, and inter-stage matching circuits.

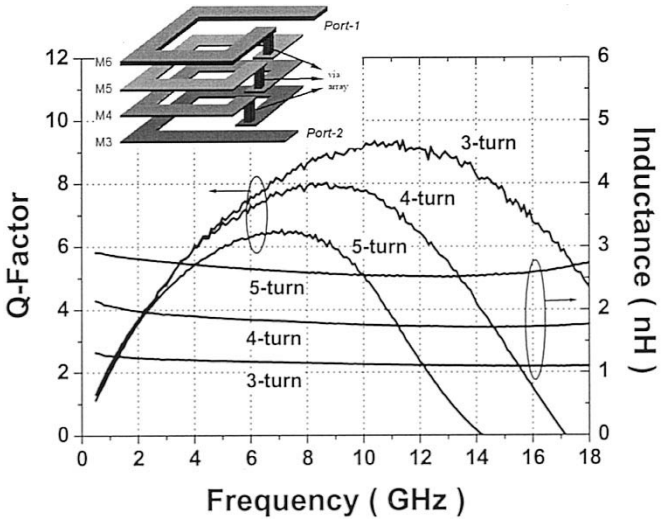

Fig. 1. Measured quality factor and inductance of helical inductors. Insert shows the 3-D view of 4-turn helical inductor. The metal width is 15 μm and the area is 90×90 μm^2.

The schematic diagram of the VCO is shown in Fig. 2(a). Both cross-coupled NMOS and PMOS pairs (M_1–M_4), in positive feedback, compensate the LC tank loss. This structure has a better phase-noise performance for a given bias current due to both higher oscillation amplitude and waveform symmetry [3]. L_x in series with the current source push to make a high impedance current source at $2f_0$ and placing a large capacitor C_x in parallel with the current source shorts noise frequencies around $2f_0$, which eliminates contribution of current source to phase noise and results in lowering phase noise [1]. In this implementation, to reduce area occupation, the noise filter was

Manuscript received March 21, 2003; revised July 18, 2003. This work was supported by the KOSEF through the MICROS Center at KAIST. The review of this letter was arranged by Associate Editor Dr. Arvind Sharma.

J. Gil, S.-S. Song, and H. Lee are with the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: jgil@kaist.ac.kr).

H. Shin is with the School of Electrical Engineering, Seoul National University, Seoul 151-742, Korea (e-mail: hcshin@snu.ac.kr).

Digital Object Identifier 10.1109/LMWC.2003.819382

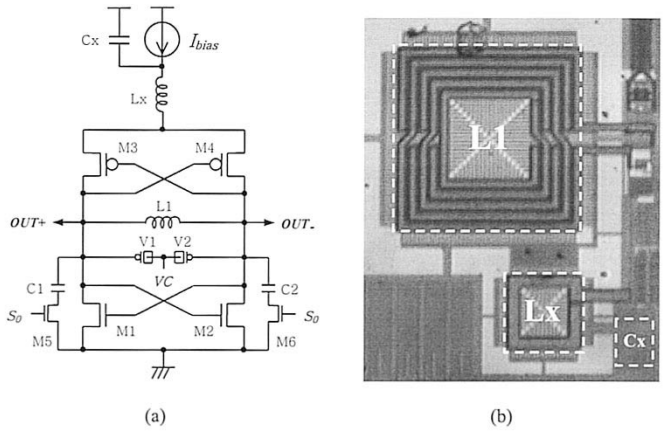

Fig. 2. (a) VCO schematic. (b) Chip photograph. The die area is 0.36×0.45 mm^2.

made of a 4-turn helical inductor (L_x) and a MOS capacitor (C_x). As shown in Fig. 2(b), the area increase due to the noise filter was very small. L_x occupied only 5% over whole chip.

The LC tank consists of one differential inductor (L_1) and two MOS varactors (V_1 and V_2). A 5.5 nH differential inductor with a poly-shield used for the tank has Q-factor at 2.5 GHz of 9. The accumulation-mode MOS varactor with n^+ poly gate in n-well [4] was used for frequency tuning. The measured capacitance varies from 104 fF to 281 fF and Q-factor is more than 60. In addition, the capacitor-switches (C_1–C_2 and M_5–M_6) for discrete frequency tuning were used to overcome process variations. The power consumption of a VCO strongly depends on the performance of the LC tank. The effective conductance of the tank was about 1.9 mS. Thus, the required transconductances of NMOS (g_{mn}) and PMOS (g_{mp}) are 5.7 mS, and the bias current ($I_{\rm bias}$) should be larger than 0.8 mA ($= 0.4$ mA $\times$ 2). In the measurement, 1.0 mA was flowed in the VCO.

We used the top-biased scheme which the current source is connected from the positive supply to the sources of the cross-coupled PMOSs. The top-biased scheme is preferred in the low-power VCO design because there is not the degradation of the negative-g_m caused by the body-effect [5]. Moreover, the top-biased scheme is more immune to substrate noise because the current source is placed in an n-well [1].

III. Measurement Results

Fig. 3(a) shows frequency-tuning characteristics and phase noise performance. The oscillator operates from 2.520 GHz to 2.651 GHz when the capacitor-switch turns off. 5.8% tuning range was obtained. Turning the capacitor-switch on, oscillation frequency shifts down. Overall tuning range at a center frequency of 2.55 GHz is 7.8%. -119.2 dBc/Hz at 1-MHz offset of phase noise was achieved. The $1/f^3$ corner of phase noise was about 120 kHz. Because the less dc current in MOSFET gives the less $1/f$ noise and also because we set $g_{mn} = g_{mp}$ for waveform symmetry, the $1/f^3$ corner of phase noise can be improved. Fig. 3(b) shows the measured output power as a function of the control voltage. Larger than -11.6 dB output power was achieved.

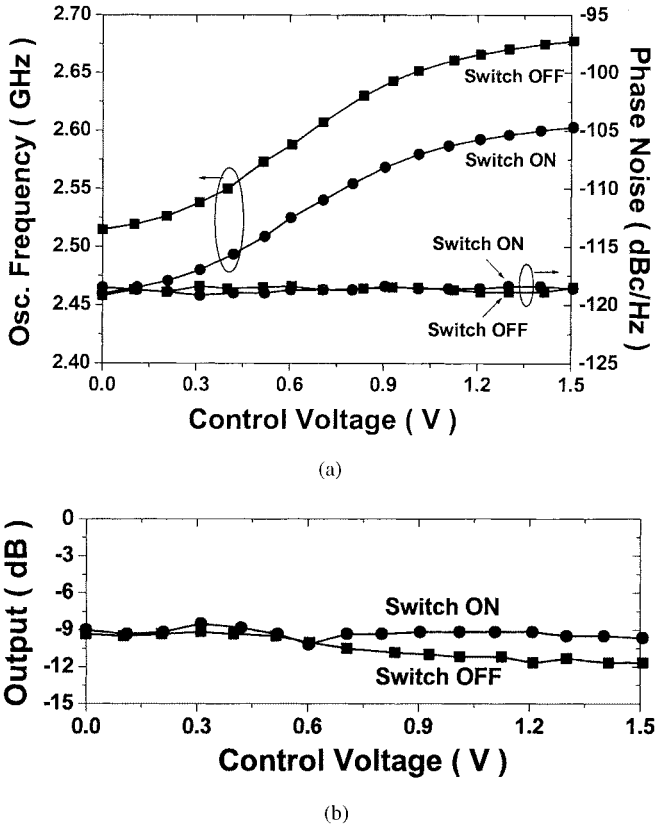

Fig. 3. (a) Measured tuning characteristics and phase noise at 1-MHz offset as a function of control voltage. (b) Measured output power.

TABLE I
Performance Comparison With Other Reported VCOs

Ref.	Technology	f_0 (GHz)	Vdd (V)	Power Diss. (mW)	Phase Noise (dBc/Hz)	Offset (MHz)	FOM (dB)	Die Area (mm^2)
This Work	CMOS 0.18μ	2.55	1.5	1.5	-119.2	1.0	185.57	0.36×0.45
[3]	CMOS 0.35μ	2.33	2.5	10.0	-121.17	0.6	182.95	NA
[5]	CMOS 0.25μ	2.4	2.0	2.8	-114.6	1.0	177.73	0.33×0.30
[6]	CMOS 0.25μ	2.36	2.5	16.25	-104.33	0.6	164.12	0.31×0.41
[7]	CMOS 0.18μ	2.45	1.8	3.6	-115.0	1.0	177.22	0.75×0.37
[8]	CMOS 0.25μ	2.4	2.5	3.75	-133.0	3.0	185.32	NA
[9]	CMOS 0.35μ	2.6	2.5	13.0	-110.0	5.0	153.18	NA
[10]	CMOS 0.35μ	2.2	1.4	12.6	-123.0	0.6	183.28	1.1×0.85
[11]	BJT	2.0	2.7	32.4	-102.0	0.1	172.92	0.60×0.60
[12]	BJT	2.4	3.6	50.0	-78.0	0.02	162.59	0.50×0.50
[13]	BJT	2.6	2.0	14.0	-104.0	0.1	180.84	NA

To compare the performance of different oscillators, figure of merit (FOM) is used as defined by [1]

$$\mathrm{FOM} = 10\log\left(\left(\frac{f_0}{f_m}\right)^2 \cdot \frac{1}{L(f_m)\cdot P}\right). \qquad (1)$$

Table I summarizes measurement results and compares to those reported in [3], [5]–[13] that are operated at 2–3 GHz band. Our VCO has the best figure-of-merit and the lowest power consumption. Also, the silicon area is quite small.

IV. Summary

A 2.5-GHz CMOS VCO with power consumption of 1.5 mW and phase noise of -119.2 dBc/Hz at 1-MHz was presented. Our VCO has the excellent performance of the phase noise over

the power consumption. In addition, we used a helical inductor as a noise filter for reducing the silicon area. Helical inductor is one of the excellent candidates for reducing the chip area.

REFERENCES

[1] E. Hegazi, H. Sjöland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1921–1930, Dec. 2001.

[2] J. Gil and H. Shin, "On-chip helical inductors for RF-ICs," *J. Korean Phys. Soc.*, vol. 40, no. 1, pp. 49–51, 2002.

[3] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, pp. 896–909, June 2001.

[4] A.-S. Porret, T. Melly, C. Enz, and E. Vittoz, "Design of high-Q varactors for low-power wireless applications using a standard CMOS process," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 337–345, 2000.

[5] J. Gil and H. Shin, "A 2.4-GHz fully integrated CMOS quadrature VCO," in *Asia-Pacific SoC Conf.*, 2002, pp. 207–210.

[6] B. Chi and B. Shi, "Integrated 2.4 GHz CMOS quadrature VCO with symmetrical spiral inductors and differential varactors," *IEEE MTT-S*, pp. 561–564, 2002.

[7] D. Leenaerts, C. Dijkmans, and M. Thompson, "A 0.18 μm CMOS 2.45 GHz, low-power quadrature VCO with 15% tuning range," *IEEE MTT-S*, pp. 67–70, 2002.

[8] D. Theil, C. Diirdodt, A. Hanke, S. Heinen, S. Waasen, D. Seippel, D. Pham-Stabner, and K. Schumacher, "A fully integrated CMOS frequency synthesizer for Bluetooth," in *Proc. IEEE RF-IC's Symp.*, 2001, pp. 103–106.

[9] C. Lam and B. Razavi, "A 2.6 GHz/5.2 GHz CMOS voltage-controlled oscillator," in *IEEE Int. Solid-State Circuits Conf.*, 1999, pp. 402–403.

[10] P. Andreani and H. Sjöland, "A 2.2 GHz CMOS VCO with inductive degeneration noise suppression," in *IEEE Custom Integrated Circuits Conf.*, 2001, pp. 197–200.

[11] M. Zannoth, B. Kolb, J. Fenk, and R. Weigel, "A fully integrated VCO at 2-GHz," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1987–1991, 1998.

[12] M. Soyuer, A. Jenkins, J. N. Burghartz, H. A. Ainspan, F. J. Canora, S. Ponnapalli, J. F. Ewen, and W. E. Pence, "A 2.4-GHz silicon bipolar oscillator with integrated resonator," *IEEE J. Solid-State Circuits*, vol. 32, pp. 268–270, 1996.

[13] C. Samori, A. Zanchi, S. Levantino, and A. L. Lacaita, "A fully-integrated low-power low-noise 2.6-GHz bipolar VCO for wireless applications," *IEEE Microwave Comp. Lett.*, vol. 11, pp. 199–201, 2001.